In the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. ~~(~~Currently amended) ~~A~~ A multilayer board, comprising:

___a ~~central~~ surface area ~~in which~~where an electrical device is ~~to be~~ mount[[~~ed~~]]able; and

___~~a localized~~ an array of capacitive elements at least partially surrounding the ~~central area~~ electrical device.

~~on the first layer or on a second layer extending parallel to the first layer.~~

2. (Currently amended) ~~The~~ The board of claim 1, wherein the capacitive elements ~~comprise capacitors~~ are ~~formed or formed~~ mounted on at least one of a first layer or a third layer and connected to a second layer.

3. (Currently amended) The board of claim 1, wherein the ~~elements~~ capacitive elements comprise at least one of capacitors or conductive ~~coplanar~~ patches ~~formed on the second layer~~.

4. (Currently amended) The board of claim 3, further comprising a C-plane ~~formed in the central area~~.

5. (Currently amended) The board of claim 4, wherein the C-plane is coplanar with the conductive patch ~~patches~~.

6. (Currently amended) The board of claim 2 [[4]], wherein [[~~the~~]] a C-plane is formed [[~~on~~]] in a ~~third~~ fourth layer extending [[~~in~~]] parallel [[~~with~~]] to the first ~~and second~~ layer ~~layers~~.

7. (Currently amended) The board of claim 3, wherein the conductive patches are

disposed adjacent to a signal line ~~disposed on the second layer~~.

8. (Currently amended) The board of claim 3, wherein a characteristic of the capacitive elements~~patches~~ in the array changes with a distance from the electrical device~~central area~~.

9. (Original) The board of claim 8 wherein the characteristic includes sizes of the patches.

10. (Original) The board of claim 8 wherein the characteristic includes shapes of the patches.

11. (Original) The board of claim 3 wherein the patches are rectangular.

12. (Currently amended) The board of claim 11, wherein the rectangular patches are larger than the electronic device and extend throughout a limited ~~the central~~ area surrounding the electrical device.

13. (Currently amended) The board of claim 3, wherein ~~further comprising a ground plane to which~~ the conductive ~~-~~patches are connected through a conductive rod ~~rods~~or a via to another conductive layer.

14. (Currently amended) The board of claim 13,[[3]] wherein at least one of the patches is [[~~are~~]] ~~-~~connected ~~to the ground plane~~ through multiple conductive rods or multiple vias.

15. (Currently amended) The board of claim [[~~2~~]] 1, wherein the capacitive elements are ~~comprise conductive coplanar patches formed on the second layer~~surface mount capacitors.

16. (Currently amended) The board of claim 1, wherein the array of capacitive

elements ~~completely~~ surrounds the ~~central~~electrical device ~~area~~.

17. (Currently amended) The board of claim 1, wherein the number of elements in the array in a first ~~the particular~~ direction from the ~~central~~ electrical device[[~~area~~]] is different from the number of elements in the array in at least one direction orthogonal to, or parallel to, the first ~~particular~~ direction from the ~~central area~~electrical device.

18. (Currently amended) The board of claim 1, wherein the capacitive elements have the same characteristics throughout the array.

19. (Currently amended) The board of claim 1, wherein multiple arrays are present in [[~~the~~]] a same layer.

20. (Currently amended) The board of claim 1, wherein a maximum of 4 elements are in the array in a [[~~the~~]] first~~particular~~ direction.

21. (Currently amended) The board of claim 14, wherein the conductive rods are plated through holes.

22. (Withdrawn) An apparatus for suppressing noise in an electrical device, the apparatus comprising: a surface on which the electrical device is to be disposed; a localized array of conductive coplanar patches adjacent to a central area over which the electrical device is to be disposed; a first conductive layer; a first dielectric layer disposed between the patches and the first conductive layer; a second dielectric layer disposed between the patches and the surface; and conductive vias extending through the first dielectric layer connecting the patches with the first conductive layer.

23. (Withdrawn) The apparatus of claim 22 wherein multiple localized arrays are arranged between the first and second dielectric layers.

24. (Withdrawn) The apparatus of claim 22 wherein the patches terminate at least one patch length from an edge of the first dielectric layer in multiple orthogonal directions.

25. (Withdrawn) The apparatus of claim 22 wherein the patches completely encircle the central area.

26. (Withdrawn) The apparatus of claim 22 wherein the patches do not completely encircle the central area.

27. (Withdrawn) The apparatus of claim 22 wherein a C-plane is disposed in the central area.

28. (Withdrawn) The apparatus of claim 22 wherein a characteristic of the patches extending from the central area in different directions are different.

29. (Withdrawn) The apparatus of claim 22 further comprising a localized array of chip capacitors disposed on the surface, the chip capacitors connected to the patches through the conductive rods, which extend through the second dielectric layer.

30. (Withdrawn) The apparatus of claim 29 wherein each patch is connected to an associated chip capacitor.

31. (Withdrawn) The apparatus of claim 22 wherein only a minimum number of patches is provided between the central area and a location on an opposite side of the localized array to provide a desired amount of attenuation of electromagnetic radiation of a desired frequency range emanating from the electrical device in a direction between the central area and the location.

32. (Withdrawn) A printed circuit board (PCB) comprising: opposing outermost

surfaces containing signal lines; an array of conductive coplanar patches disposed between the surfaces; a first conductive layer; a first dielectric layer disposed between the patches and the first conductive layer; a second conductive layer having a different potential than the first conductive layer; a second dielectric layer disposed between the patches and the second conductive layer; and conductive rods extending through the first dielectric layer connecting the patches with the first conductive layer such that the patches are at the same potential as the first conductive layer and the second conductive layer is more proximate to the patches than the first conductive layer.

33. (Withdrawn) The PCB of claim 32 wherein the patches are disposed closer to the second conductive layer than any other non-dielectric layer.

34. (Withdrawn) The PCB of claim 32 further comprising: a third conductive layer disposed on an opposite side of the second conductive layer as the patches; and a third dielectric layer disposed between the second and third conductive layers.

35. (Withdrawn) The PCB of claim 34 wherein the first and third conductive layers are more proximate to the outermost surfaces than any other conductive layer.

36. (Withdrawn) The PCB of claim 34 wherein the first and third conductive layers are at the same potential.

37. (Withdrawn) The PCB of claim 36 wherein the first and third conductive layers are grounded.

38. (Withdrawn) The PCB of claim 32 further comprising an inner layer on which signal lines are arranged, the inner layer disposed between the first and second conductive layers, wherein the patches are disposed on the inner layer.

39. (Withdrawn) The PCB of claim 38 further comprising another first conductive

layer, another inner layer containing signal lines and an array of patches connected with the other first conductive layer, and another second conductive layer at a different potential from the other first conductive layer, wherein the other first conductive layer, the other inner layer, and the other second conductive layer are disposed substantially mirror image around a center of the PCB from the first conductive layer, the inner layer, and the second conductive layer, respectively.

40. (Withdrawn) The PCB of claim 32 further comprising an inner layer on which signal lines are arranged, the inner layer disposed between the first conductive layer and the patches, wherein the conductive rods extend through the inner layer without contacting the signal lines.

41. (Withdrawn) The PCB of claim 40 further comprising another first conductive layer, another inner layer containing signal lines, another array of patches connected with the other first conductive layer, and another second conductive layer at a different potential from the other first conductive layer, wherein the other first conductive layer, the other inner layer, the other array of patches and the other second conductive layer are disposed substantially mirror image around a center of the PCB from the first conductive layer, the inner layer, the localized array of patches, and the second conductive layer, respectively.

42. (Withdrawn) The PCB of claim 40 wherein the patches are disposed closer to the second conductive layer than any other non-dielectric layer.

43. (Withdrawn) The PCB of claim 32 further comprising: a third conductive layer disposed on an opposite side of the first conductive layer as the patches; and an inner layer on which signal lines are arranged, the inner layer disposed between the first and third conductive layers.

44. (Withdrawn) The PCB of claim 43 wherein the first and third conductive layers are at the same potential.

45. (Withdrawn) The PCB of claim 44 wherein the first and third conductive layers are grounded.

46. (Withdrawn) The PCB of claim 43 further comprising another first conductive layer, another inner layer containing signal lines, another array of patches connected with the other first conductive layer, another second conductive layer at a different potential from the other first conductive layer, and another third conductive layer, wherein the other first conductive layer, the other inner layer, the other array of patches, the other second conductive layer and the other third conductive layer are disposed substantially mirror image around a center of the PCB from the first conductive layer, the inner layer, the localized array of patches, the second conductive layer and the third conductive layer, respectively.

47. (Withdrawn) The PCB of claim 43 wherein the patches are disposed closer to the second conductive layer than any other non-dielectric layer.

48. (Withdrawn) The PCB of claim 32 further comprising a plurality of inner layers on which signal lines are arranged, the inner layer disposed between the first and second conductive layers.

49. (Withdrawn) The PCB of claim 48 wherein the patches are disposed on one of the inner layers.

50. (Withdrawn) The PCB of claim 48 wherein the inner layers are disposed between the first conductive layer and the patches, the conductive rods extend through the inner layers without contacting the signal lines.

51. (Withdrawn) The PCB of claim 48 wherein the patches are disposed closer to the second conductive layer than any other non-dielectric layer.

52. (Withdrawn) The PCB of claim 32 wherein at least one of the first and second conductive layers are split into coplanar split portions such that different potentials are applied to the split portions.

53. (Withdrawn) The PCB of claim 32 wherein the first conductive layer is a power plane and the second conductive layer is a ground plane.

54. (Withdrawn) The PCB of claim 32 wherein the patches are coplanar with a C-plane.

55. (Withdrawn) The PCB of claim 32 wherein the patches are formed in a localized array arranged such that the patches in the array cover an area substantially less than that of the PCB

56. (Withdrawn) A method of attenuating electromagnetic radiation in a particular direction along a printed circuit board (PCB), the method comprising providing a localized array of elements between two coplanar locations of the PCB and limiting a number of unit cells of the array to substantially fewer than a number of unit cells to cover an entire distance between the coplanar locations.

57. (Withdrawn) The method of claim 56 wherein the elements comprise conductive coplanar patches between surfaces of the PCB.

58. (Withdrawn) The method of claim 57 further comprising providing a C-plane that is coplanar with the patches.

59. (Withdrawn) The method of claim 56 wherein the elements comprise chip capacitors disposed on a surface of the PCB.

60. (New) The board of claim 2, wherein the capacitive elements are connected to another layer by an inductive element.

61. (New) The board of claim 60, wherein the inductive element is a conductive rod or a via.

62. (New) The board of claim 3, wherein the conductive patch is connected to at least one of the first layer or the second layer.

63. (New) The board of claim 3, wherein the conductive patch is connected by an inductive element.

64. (New) The board of claim 63, wherein the inductive element is a conductive rod or a via.

65. (New) The board of claim 3, wherein a third layer is disposed between the first layer and the second layer.

66.(New) The board of claim 1, wherein the capacitive elements are formed or mounted on a second layer and connected to a first layer.

67. (New) The board of claim 1 wherein the surface area is coplanar with a conductive layer.

68. (New) The board of claim 3, wherein the conductive patches are disposed closer to the surface area than to any other non-dielectric layer.